In the claims:

Please substitute the following full listing of claims for the original claim listing.

1. (Original) A method of forming bitline contacts, the method comprising:

forming gate conductor lines with a capping layer on a substrate;

depositing an oxide layer over the capping layer;

forming a bitline contact line mask over portions of the oxide layer;

etching the bitline contact line mask to the capping layer and between the gate conductor lines stopping at the substrate;

depositing a silicon layer on the substrate between the conductor lines and non etched portions of the oxide layer;

depositing a bitline layer on the silicon layer;

masking and etching portions of the bitline layer; and

depositing metal over the silicon layer and on sides of non etched portions of the bitline layer to form left and right bitlines.

2. (Original) The method of claim 1, wherein a layer of BoroPhosphoSilicate Glass (BPSG) is deposited over the capping layer prior to the deposition of the oxide layer.

3. (Original) The method of claim 2, further comprising annealing the BPSG layer.

4. (Original) The method of claim 3, further comprising planarizing the BPSG layer to below tops of the gate conductor lines.

5. (Original) The method of claim 1, wherein the oxide layer is a TEOS layer.

6. (Original) The method of claim 5, further comprising planarizing the TEOS layer prior to forming the bitline contact line mask.

7. (Original) The method of claim 1, further comprising forming spacers between adjacent gate conductor lines.

8. (Original) The method of claim 7, further comprising depositing a layer of BoroPhosphoSilicate Glass (BPSG) over the capping layer wherein the etching of the oxide and BPSG selective to the capping layer and selective to the spacers.

9. (Original) The method of claim 1, wherein the silicon layer is an n+ amorphous/polysilicon layer.

10. (Original) The method of claim 9, wherein the n+ amorphous/polysilicon layer is selectively etched or polished back to the oxide layer, the oxide layer being a TEOS layer.

11. (Original) The method of claim 10, further comprising etching the n+ amorphous/polysilicon layer to below tops of the gate conductor lines and below the oxide layer.

12. (Original) The method of claim 11, further comprising planarizing the bitline layer, the bitline layer being a TEOS layer.

13. (Original) The method of claim 1, wherein the etching of the bitline stops at the non etched portions of the oxide layer.

14. (Original) The method of claim 1, wherein the oxide layer is etched to the silicon layer selective to the capping layer encapsulating the gate conductor lines.

15. (Original) The method of claim 1, further comprising forming insulating sidewalls on the gate conductor lines.

16. (Original) The method of claim 15, wherein the insulating materials is silicon nitride.

17. (Original) The method claim 16, further comprising depositing a conformal silicon nitride layer on the gate conductor lines and active areas and isolation areas between the active areas.

18. (Original) The method of claim 1, wherein an isotropic dry etch is used to recess the silicon layer to below a level of the capping layer.

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Cancelled)

28. (Cancelled)